A MOSFET Power Amplifier with Error Correction*

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Power MOSFETs are emerging as the device of choice for high-quality power amplifiers because of their speed, reduced need for protection, and falling cost. A low-distortion power amplifier design is presented which includes output stage error correction to reduce the effect of transconductance droop in the crossover region and thus allow operation at more efficient bias levels.

0 INTRODUCTION

The rapid evolution of power MOSFETs during the last few years has brought them to the point where they are now very attractive for use in audio amplifier power output stages. Important improvements include increased voltage, current, and dissipation ratings, reduced "on" resistance, availability of complementary pairs, and greatly reduced cost. Although a 75-W MOSFET is still more expensive than a 150-W bipolar transistor, the premium is small when considered relative to total amplifier cost and improved performance.

The purpose of this paper is to demonstrate the level of performance achievable with current technology and to illustrate practical circuit techniques for achieving this performance.

Power MOSFETs have several fundamental advantages over bipolar power transistors, most notably speed and freedom from secondary breakdown. The latter provides higher "usable" power dissipation, improved reliability, and freedom from safe-area limiter circuits, which can misbehave and cause audible degradation. MOSFETs also have some disadvantages in comparison with bipolar transistors. These include higher turn-on voltage drive requirements and smaller transconductance at low current levels. The former tends to contradict generalizations that have been made to the effect that drive circuits for power MOSFETs are less expensive, at least for the reliable source–follower configuration. The latter results in transconductance droop in the crossover region if bias currents are not fairly high. Such transconductance droop can result in crossover distortion.

In this paper we present a high-performance amplifier design which utilizes the advantages of the power MOSFET while dealing with the drawbacks of the device. Although not taken to an extreme, the underlying philosophy of the design is that small-signal silicon is inexpensive, that is, that the overwhelming portion of expense in a power amplifier is in items like the power transformer, filter capacitors, power transistors, heat sinks, chassis, and related hardware. Thus, in order to take full advantage of the performance achievable with the MOSFET output stage, a very-high-quality front end and driver are provided. The driver, operating from regulated boosted supplies, is capable of providing high voltage and current swings to the power MOSFETs with good headroom. Output stage transconductance droop is dealt with by employing a simple but very effective output stage error-correction technique proposed by Hawksford [1]. The resulting design achieves a 20-kHz total harmonic distortion figure of less than 0.0015% at an idle bias of only 150 mA.

1 APPLYING POWER MOSFETS

The design of MOSFET power amplifiers is quite straightforward and conventional as long as differences between MOSFETs and bipolar transistors are understood. In this section we review current MOSFET technology, compare MOSFET and bipolar characteristics, and focus on several important design considerations.

1.1 Power MOSFET Structures

Power FET technology has evolved over the last 15 years from JFET to MOSFET devices with many different structures along the way. The modern power

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MOSFET is made possible by many of the same advanced techniques that are employed in MOS large-scale integrated circuits, including fine-line photolithography, self-aligned polysilicon gates, and ion implantation. Two planar structures, one lateral MOSFET and one vertical DMOS, are currently the most suitable devices for audio applications. Both are readily available in complementary pairs, offer suitable current and voltage ratings, and are realized with a cellular structure which provides the equivalent of thousands of small-geometry MOSFETs connected in parallel. Another DMOS structure, the nonplanar V-groove power MOSFET, still enjoys considerable popularity, but limited availability of *p*-channel versions with suitable voltage, current, and "on" resistance makes them less attractive for audio output stages.

The structure of the lateral power MOSFET is illustrated in Fig. 1(a) [2]. The *n*-channel device shown is similar to small-signal MOSFETs found in integrated circuits, except that a lightly doped *n*-type drift region is placed between the gate and the n^+ drain contact to increase the drain-to-source breakdown voltage by decreasing the gradient of the electric field. Current flows laterally from drain to source when a positive bias on the silicon gate inverts the *p*-type body region to form a conducting *n*-type channel. (Note that the arrows in Fig. 1(a) and (b) illustrate the direction of carrier flow rather than conventional current flow.) The device is fabricated by a self-aligned process where the source and drain (drift region) diffusions are made using the previously formed gate as part of the mask. Alignment of the gate with the source and drain diffusions thus occurs naturally, and the channel length is equal to the gate length less the sum of the out-diffusion distances of the source and drain regions under the gate. Small gate structures are thus required to produce the short channels needed to realize high transconductance and low "on" resistance.

While providing high breakdown voltage, the lightly doped drift region tends to increase "on" resistance. This partly explains why higher voltage power MOSFETs tend to have higher "on" resistance. A further disadvantage of this structure is that all of the source, gate, and drain interconnect lies on the surface, resulting in a fairly large chip area for a given amount of active channel area, which in turn limits transconductance per unit area. Series gate resistance also tends to be fairly high (about 40 Ω) as a result, limiting maximum device speed. The lateral power MOSFETs are presently the most widely used MOSFET in audio amplifiers. Examples of this structure are the Hitachi 2SK-134 (*n*-channel) and 2SJ-49 (*p*-channel). Desirable features of these devices include a threshold voltage of only a few tenths of a volt and a zero temperature coefficient of drain current versus gate voltage at a drain current of about 100 mA, providing good bias stability.

A more advanced power MOSFET design is the vertical DMOS structure illustrated in Figure 1(b) [2]. When a positive gate bias inverts the *p*-type body region into a conducting *n* channel, current initially flows *vertically* from the drain contact on the back of the chip through the lightly doped *n*-type drift region to the channel, where it then flows laterally through the channel to the source contact. The doubly diffused structure is formed by starting with an *n*-type wafer with a lightly doped epitaxial layer. The *p*-type body region and the n^+ source contact are then diffused into the wafer in that order. Because both diffusions use the same mask edge on either side of the gate, channel length is the difference of the out-diffusion distances of the body and source regions. As a result, extremely short channels are easily realized without heavy dependence on photolithographic resolution. This results in high transconductance and low "on" resistance. The geometry and dimensions of the *n*-type drift region are such that its effective resistance can be much smaller than that of the drift region for the lateral devices. This also aids in achieving low "on" resistance while retaining high voltage capability.

The vertical DMOS structure is much more compact and area-efficient than the lateral structure because the source metallization covers the entire surface; the polysilicon gate interconnect is buried under the source metallization. Also, each gate provides two channels, one on each side. The amount of active channel area for a given chip area is thus higher than for the lateral geometry. The fact that source and drain metallizations can each occupy virtually an entire side of the chip leads to high current capability. Finally, the length of the gate can be greater in this structure because it does not directly control channel length. This, combined with the compact structure, results in lower series gate resistance (about 6 Ω) and higher speed. Because of its many advantages, the planar vertical DMOS structure is now the main-line power MOSFET technology. Examples of this structure are the International Rectifier IRF-132 (*n*-channel) and IRF-9130 (*p*-channel), whose cellular structure is illustrated in Fig. 1(c) [3]. These are the devices used in the amplifier to be described.

1.2 Transfer Characteristics

Fig. 2 shows the drain and gate transfer characteristics typical of the devices used in this project [3]. The important point to see here is that these enhancement devices require about 3 V of forward gate bias to begin to turn on (e.g., gate threshold voltage V_t) and may require as much as 10 V to conduct high currents (12 A). The maximum transconductance of the power MOSFETs, on the order of 2–5 siemens (S), is considerably less than that of a bipolar transistor; this also contributes to the higher voltage drive requirement.

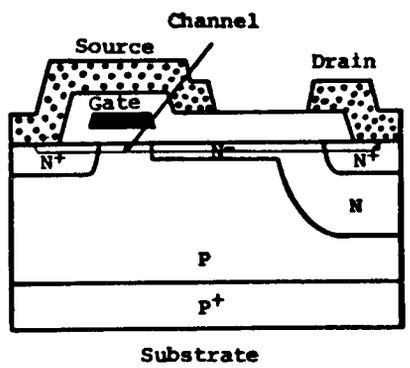
While the required bias voltage is thus higher than for bipolar transistors, it can still be generated by the traditional V_{be} multiplier circuit. As will be seen in Section 1.3, however, conditions for achieving thermal bias stability are considerably relaxed.

If the popular source–follower output stage configuration is used, the substantial gate drive voltage required for high currents means that the driver stage

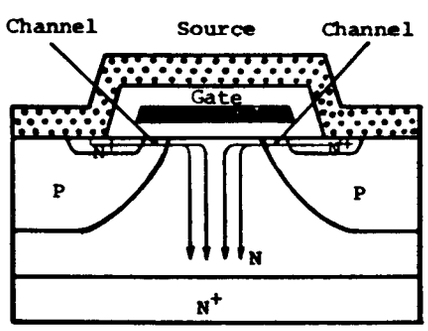
should be provided with a boosted power supply voltage, greater than that of the main high-current supply, in order to take full advantage of the voltage swing available from the latter. The current requirements for the boosted supply are small, and it can be regulated at little additional expense, thus reducing hum, crosstalk, and modulation distortion. Several high-quality bipolar power amplifiers also use boosted driver supplies, some regulated.

1.3 Biasing and Thermal Stability

Modern complementary MOSFETs, with maximum "on" resistances of only about 0.3 Ω, are almost as efficient as bipolar transistors in terms of voltage dropped from supply rail to load in output stages. However, they typically require a higher operating current to achieve a given transconductance. This characteristic is illustrated in Fig. 3. The device transconductance in a source–follower or emitter–follower output stage is important because it determines the small signal voltage drop through the stage as a function of current. This is especially important in class AB stages where it is desirable that the sum of the effective transconductances of both halves be high and be constant with current so as to avoid crossover distortion. It can be seen from Fig. 3 that approaching this condition with power MOSFETs requires fairly substantial bias current (as a rough starting point, that current where transconductance is one-half its high-current asymptotic value), on the order of a few hundred milliamperes.



(a)



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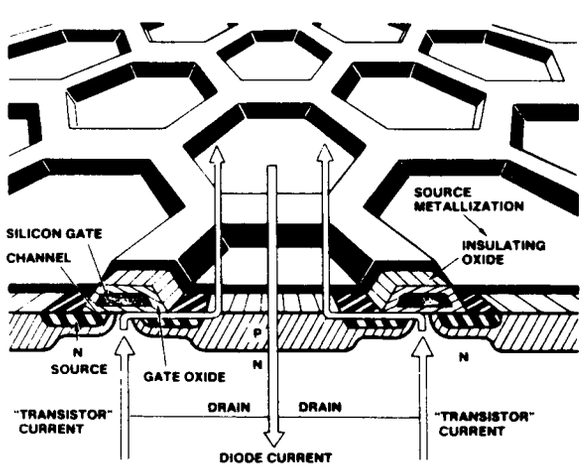


(c)

Fig. 1. Power MOSFET structures. (a) Lateral [2]. (b) Vertical DMOS [2]. (c) Cellular layout of International Rectifier HEXFET vertical DMOS transistor [3].

In contrast, bipolar power transistors are typically biased at a much lower current, but this is not entirely advantageous. A typical bipolar output stage will often be biased approximately where the dynamic emitter resistance of the output devices ($1/g_m$) at crossover is equal to the associated ballast resistance as a compromise in achieving approximately constant total output stage transconductance as a function of current. This is done because both halves are on and contribute transconductance in the crossover region, while only one-half contributes transconductance at currents well outside the crossover region. This often results in bias currents of less than 100 mA per output transistor, sometimes as low as 20 mA. This small amount of bias current compared to several amperes of signal current being handled can sometimes result in unexpected temporary bias inadequacy, resulting in crossover distortion, because a small change in circuit parameters (about 50 mV) can cause the bias current to vary considerably. Bipolar output stages can be operated in an overbiased mode, but the penalty can be dangerously reduced thermal stability if larger heat sinks are not used, or increased crossover distortion if larger ballast resistors are used. Compared to bipolar designs, class AB MOSFET power output stages tend to have a wider class A region of operation (because of their higher bias current) and a smoother transition to the class B region of operation.

Because of their relatively strong negative temperature coefficient of base–emitter voltage for a fixed collector current, bipolar transistors in output stages require a thermal feedback loop and emitter ballast resistors to stabilize bias over temperature changes. The bias voltage is usually generated by several forward-biased junction voltage drops, some portion of which is placed on the heat sink to provide the thermal feedback. As the heat sink gets hotter, the bias voltage decreases, providing stabilization. The percentage of the bias derived from the heat sink reference is important. If it is too small, the bias will be undercompensated, and the amplifier will be overbiased when the heat sink is hot as a result of large program signals. Conversely, if the percentage is too large, the amplifier will be overcompensated and will be underbiased fol-

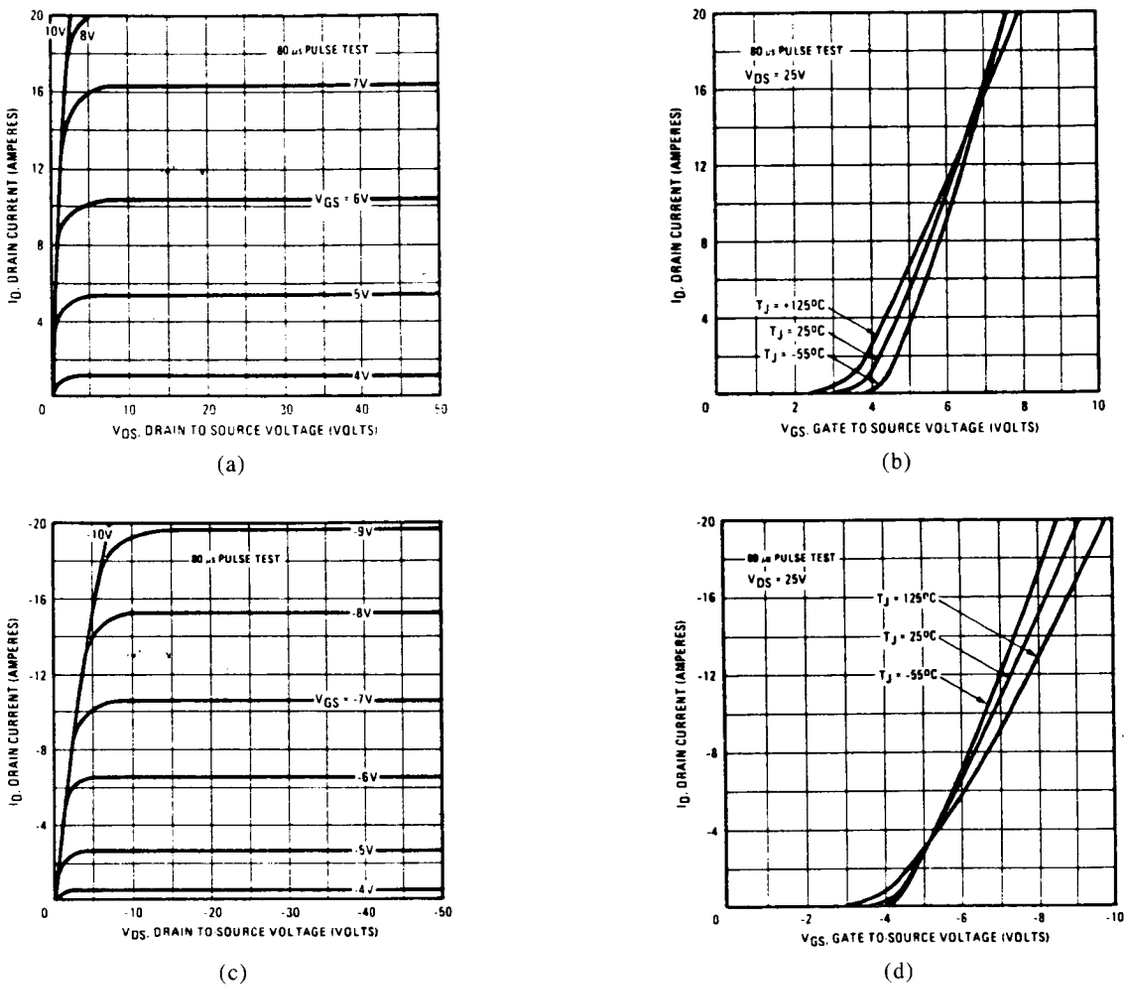


Fig. 2. Drain and gate characteristics for power MOSFET types. (a), (b) IRF-132. (c), (d) IRF-9130.

lowing a high-dissipation interval.

Unfortunately the sensing junction on the heat sink is usually not at the actual junction temperature of the power devices. Thermal attenuation, low-pass filtering, and delay exist between the power junctions and the sensor, resulting in a high-order feedback loop whose thermal transient response is not always well damped. At best, bias will only be correct on the average; it will not track fast program-induced thermal differences between the power junctions and the heat sink [4]. The exercise of adjusting for optimum bias under static conditions is thus relatively ineffective.

Thermal bias stability for the power MOSFETs is much better than that for bipolar transistors, even though the vertical DMOS devices have a V_{gs} temperature coefficient of about −5.0 mV/°C at a typical bias current of 150 mA. The difference can be seen by evaluating the thermal sensitivity S_{TH}, here defined as the fractional change in collector or drain current per °C rise in case temperature with a fixed base or gate voltage.

$$S_{TH} = \frac{TC_v \cdot g_m}{I_b}$$

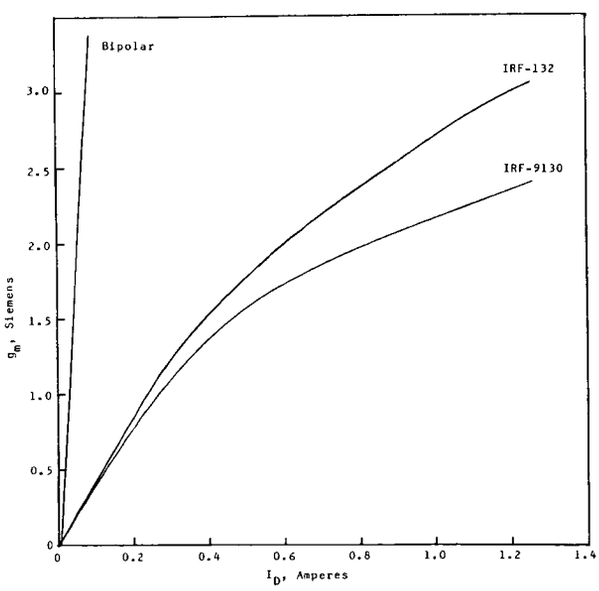


Fig. 3. Power MOSFET transconductance versus drain current. For comparison, note much greater ratio of transconductance to operating current typical of bipolar transistors.

where TC_v is the base or gate voltage temperature coefficient for constant collector or drain current, g_m is the stage transconductance (including the effect of emitter ballast resistors if present), and I_b is the nominal bias current. For a bipolar design biased at 80 mA with 0.33-Ω emitter resistors, S_{TH} = 0.042/°C. For a MOSFET stage biased at 150 mA with no source resistors and a device transconductance of 0.5 S, S_{TH} = 0.017/°C, better by a factor of 2.5.

Thermal bias stability of an amplifier can be evaluated by running it at one-third rated power into an 8-Ω resistive load for 10 min and then plotting the measured bias current as a function of time after the signal and load are removed. This will provide the equivalent of a step response for the thermal feedback loop. Fig. 4 presents the results of such an exercise for four amplifier designs: an undercompensated bipolar, an overcompensated bipolar, an uncompensated MOSFET, and the slightly overcompensated MOSFET design to be presented in Section 2. All of the amplifiers had identical rail voltages, power ratings (50 W) and heat sinks.

The first 10 s illustrate the effect of the faster power transistor thermal time constant, while the remaining time illustrates the heat sink time constant. Notice that both bipolar cases are actually very overbiased during and immediately following the high-dissipation "program" interval because the power junctions run hotter than the heat sink due to thermal resistance from junction to heat sink. Overcompensation cannot reduce this effectively and will result in a seriously underbiased condition at other times. In comparison, the compensated MOSFET design has much greater short-term and long-term thermal bias stability. Even the uncompensated MOSFET design has better thermal performance than the bipolar designs, suggesting that smaller vertical DMOS amplifiers (say, below 50 W) with good heat sinking can probably be made without thermal feedback. The lateral power MOSFETs mentioned in Section 1.1 appear not to require thermal feedback under any normal conditions.

1.4 Paralleling Power MOSFETs

While bipolar transistors are regularly placed in parallel with small individual emitter ballast resistors, the paralleling issue is not as straightforward for power MOSFETs, at least in linear applications. It has been said that the negative temperature coefficients of transconductance and "on" resistance of MOSFETs act to suppress current hogging by one transistor, thus permitting easy paralleling of MOSFETs without ballast resistors. This appears to be true for hard-switching applications where the paralleled devices are all fully turned on together (i.e., channels fully enhanced by forward gate voltage) so that current and dissipation imbalances are only a result of mismatched "on" resistance.

However, the issue is more complex for linear, and especially low-distortion, applications because the operating region of interest is not the fully turned on region, but rather the linear region wherein drain current at a specified gate voltage is important. Specifically, recognizing that the gate threshold voltage specification for these devices is 2–4 V, an examination of the gate transfer characteristics of Fig. 2 indicates that a very serious current imbalance can exist unless gate threshold voltages among paralleled devices are reasonably matched. It is also apparent that reasonable temperature differentials will not adequately reduce the imbalance. This is especially true if a common heat sink is employed. Because of the size of the worst case threshold voltage differentials possible, source ballast resistors are not a reasonable approach to achieving balance.

It thus appears that for high-quality audio applications where paralleled devices are necessary, both threshold voltage and transconductance of paralleled devices should be matched. Matching that guarantees that all devices are carrying ±50% of their nominal current share in the quiescent bias state, and ±25% of their share at high currents is probably adequate. For the IR devices used here, V_{GS} matching of ±0.1V at 50 mA and ±0.25V at 4 A will typically satisfy this matching criterion.

1.5 Speed and Input Capacitance

Power MOSFETs tend to be inherently faster than bipolars, partly because there are no minority carrier effects. Their speed is primarily limited by the ability of the drive circuitry to charge the internal gate electrode capacitance through the effective gate resistance. With 7 Ω of gate resistance and 700 pF of gate–source (input) capacitance (typical values), transconductance for these devices is down 3 dB at about 32 MHz. Another important measure of speed is transconductance divided by input capacitance; when multiplied by 2π, this is essentially the f_t for a bipolar transistor. For these power MOSFETs operating at 1 A with a transconductance of 1.5 S, this figure is 341 MHz.

The wider bandwidth, reduced excess phase, and reduced variation of device speed with voltage and current tend to allow greater high-frequency negative

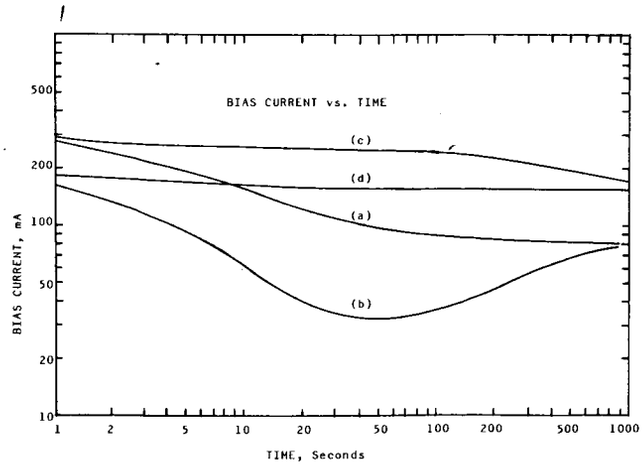


Fig. 4. Output stage bias current as a function of time after removal of signal and load, illustrating thermal bias stability. (a)—undercompensated bipolar; (b)—overcompensated bipolar; (c)—uncompensated vertical DMOS; (d)—slightly overcompensated vertical DMOS.

feedback with greater stability. The higher switching speed also tends to reduce dynamic crossover distortion. The MOSFET's higher switching speed also greatly reduces the flow of class AB common-mode current at high frequencies, which poses such a destructive threat to many bipolar designs.

Although power MOSFETs require virtually no drive current at low frequencies, their substantial input capacitance means that drive circuits with forward and reverse drive capabilities similar to those employed for bipolar output stages should be used for wideband high-slew-rate circuits in demanding audio applications. Although the gate–source capacitance can be on the order of 700 pF, this capacitance is effectively "bootstrapped" in a source-follower output stage, typically reducing its effect by about an order of magnitude. The smaller gate–drain capacitance, about 100 pF, is also present. A 100-V/μs slope with an effective capacitance of 170 pF thus requires a 17-mA current capability from each driver.

1.6 Parasitic Oscillations

Power MOSFETs are much faster than bipolar power transistors, and as a result are much more prone to very-high-frequency parasitic oscillations. When combined with (or part of) a resonant circuit, power MOSFETs have more than enough gain to sustain oscillations at resonance in the 20–100-MHz frequency range. Parasitic oscillations are likely because high-Q resonant circuits are easily formed by combinations of lead inductance and device capacitances at these frequencies. For example, a 1-in (25-mm) length of wire has an inductance on the order of 0.02 μH. This will resonate with the 700-pF gate–source capacitance of a MOSFET at only 42 MHz. Fig. 5 shows a highly simplified power MOSFET model and two of the many oscillator topologies which can be formed by a source-follower configuration. The substantial drain–source capacitance aids formation of the Colpitts topology; the analogous collector–emitter capacitance in bipolar transistors is usually quite small.

Close bypassing and minimization of lead inductance alone are usually insufficient to eliminate parasitic oscillations. These techniques are extremely important, however, because they drive the resonant frequencies

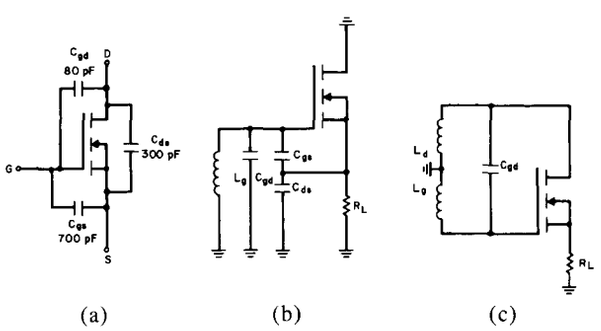


Fig. 5. Power MOSFET parasitic oscillation models. (a) Important MOSFET device capacitances. (b) Colpitts oscillator formation. (c) Modified Hartley oscillator formation.

up to a region where they are more easily damped by introducing a reasonable amount of loss. Such loss is most often introduced with a small resistor (typically 50–500 Ω) in series with the gate of each power MOSFET. Unfortunately this resistor, in combination with the gate–source capacitance, degrades the speed of the power MOSFET. The challenge is to eliminate the parasitic oscillations without giving up too much speed. Ferrite beads in the gate or drain leads can also be effective.

Paralleling of power MOSFETs can increase the tendency to parasitic oscillation because more active and reactive elements are being added to the system, increasing the opportunities for formation of an efficient oscillator [5]. The techniques for avoiding oscillations in this situation are, however, the same as for the non-paralleled case. Loss elements are applied individually to each power MOSFET.

Parasitic oscillations do not merely create distortion and radio-frequency interference. They are one of the most destructive forces facing the otherwise robust power MOSFET. The most serious threat is the large gate–source voltage excursions that can occur under some conditions, breaking down the thin gate oxide (typically rated at 20 V) and destroying the device.

1.7 Safe Operating Area

Perhaps one of the most important advantages of power MOSFETs for audio use is their freedom from secondary breakdown, which results in a large safe operating area (SOA). A highly simplified explanation of secondary breakdown in bipolar transistors is that it results from localized current hogging, which in turn results from localized thermal "hot spots." Transistor current at a given base–emitter voltage has a very strong positive temperature coefficient. Thus a hot spot carries more current and gets even hotter as a result. This regenerative process, once started, can be very rapid and unforgiving. It can persist even after the external voltage and current conditions re-enter the safe operating area, leading to destruction.

The relationships in a power MOSFET are in contrast *degenerative* in nature because hotter regions exhibit reduced transconductance and thus tend to conduct less of the total current. This tends to equalize the temperature across the chip. The safe area of a MOSFET is thus primarily governed by simple thermal considerations of how much energy (product of power and time) is required to raise the temperature of the hottest point on the chip (which will not be much different than the average temperature of the whole chip) to a dangerous point.

Fig. 6 shows a comparison of the safe operating areas for a power MOSFET and a typical bipolar power transistor. Notice that there are no steep secondary breakdown SOA slopes at high voltages for the MOSFET; it is essentially limited by simple power dissipation over its full voltage range. This is also true for short-term dissipation well in excess of rated continuous dissipation, where thermal time constants govern the al-

lowable excess dissipation. For example, a 25-A peak with 100 V across the MOSFET can be handled for 10 μs. Fig. 6 illustrates that "usable" dissipation (safe operating area at higher voltages) for a MOSFET may be equal to that of a bipolar power transistor of substantially higher rated power dissipation. The safe operating area at high voltages is particularly important when difficult reactive loads are being driven. In many power amplifiers the use of multiple paralleled output devices is for reasons of increased safe operating area rather than simple thermal considerations. Finally, freedom from secondary breakdown means freedom from complex safe-area limiter circuits, some of which are notorious for their misbehavior [6].

The methods employed for specifying the safe operating area for bipolar and MOSFET power transistors are also usually different, suggesting even greater relative ruggedness for power MOSFETs under transient or fault conditions. While manufacturers usually determine bipolar transistor safe operating area by destructive testing followed by the addition of some safety margin, the power MOSFET safe operating area is typically specified by employing calculations of transient thermal impedance to define voltage–current–time conditions which limit transient junction temperature to the rated continuous value (usually 150°C). The rated junction temperature for power MOSFETs is, however, primarily governed by concern about long-term metal migration effects and is nowhere near destruction on a short-term basis (Hitachi indicates that the destruct temperature is more like 300°C [2]). Published short-term SOA curves for power MOSFETs are thus quite conservative as long as excursions outside the region are infrequent. This is the primary reason why only very simple protection circuits (i.e., fuses or relays) are usually adequate for power MOSFET amplifiers.

1.8 A Simple MOSFET Power Amplifier

Fig. 7 illustrates a simple 50-W MOSFET power amplifier design. It is notably similar to what a simple bipolar power amplifier design would look like. Transistors Q_1 and Q_2 comprise the input differential amplifier whose output is converted to a single-ended current by current mirror $Q_{3,4}$. This current feeds the common-emitter predriver Q_5, which is provided with a constant-current load. Capacitor C_1 provides Miller-effect feedback compensation and establishes a stable gain crossover frequency of approximately 2 MHz. Transistor Q_6 is connected in a conventional V_{be} multiplier circuit to provide adjustable bias (nominally about 8 V) for the output stage. As mentioned in Section 1.3, smaller amplifiers with ample heat sink area may not need to employ thermal feedback in the bias circuit. Where thermal feedback is required, a heat-sink-mounted sensing diode can be placed directly in series with the emitter of Q_6 if the associated resistor values are modified appropriately. In most cases this will provide approximately the correct degree of compensation. Emitter–follower drivers Q_7 and Q_8 provide a low-impedance drive for the gates of power MOSFETs Q_9 and Q_{10}. The drivers isolate the high-impedance predriver collector circuit from the nonlinear input capacitance of the MOSFETs and provide adequate charge and discharge current for the MOSFET gate circuits. The boosted supplies for all circuits prior to the output stage enable the drive circuitry to provide adequate gate voltage to fully turn on the MOSFETs while maintaining margin against saturation. Zener diodes D_1–D_4 protect the MOSFETs from excessive gate–source voltages of either polarity.

2 A HIGH-PERFORMANCE MOSFET POWER AMPLIFIER

In this section a practical high-performance MOSFET power amplifier design is presented which incorporates the principles of Section 1 and includes open-loop error correction in the output stage. The amplifier demonstrates the kind of performance achievable when modern power MOSFETs are combined with high-performance circuit techniques.

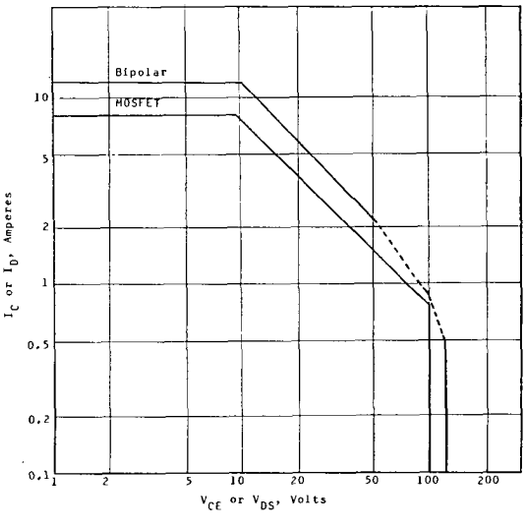


Fig. 6. Safe operating area (SOA) comparison of bipolar ring-emitter transistor (2SA-1072) and a power MOSFET (IRF-9130). Rated power dissipations are 120 W and 75 W, respectively.

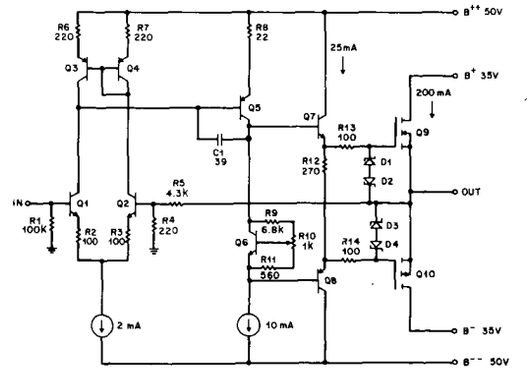


Fig. 7. Simple MOSFET power amplifier. Note use of boosted supplies for driver circuitry to satisfy power MOSFET gate drive requirements.

2.1 Input and Driver Circuits

As would be the case with a bipolar design as well, many improvements can be made to the front end of the simplified amplifier of Fig. 7 in order to provide higher performance and take full advantage of the capability of the MOSFET output stage. Although substantially adding to the complexity of the schematic in appearance, such improvements primarily involve only small-signal, low-voltage transistors and inexpensive passive components, and thus contribute only a small percentage increase to total amplifier cost.

The front end for the amplifier to be discussed here is shown in in Fig. 8. The input stage is a differential JFET-bipolar cascode with a constant current bias supply. The cascode allows the use of a low-noise dual JFET, achieving a referred input noise of less than 6 $\eta V/\sqrt{Hz}$. It also provides good common-mode and power supply rejection, necessary because negative feedback is not very effective in reducing power supply and common-mode impairments introduced at the input stage. The degenerated JFET input stage can handle fairly large open-loop input signals with relatively low distortion, making the amplifier relatively immune to transient intermodulation distortion (TIM) and radio-frequency interference effects.

The input stage is loaded by current sources (Q_6, Q_7) to provide high open-loop gain at low frequencies. Emitter–followers Q_8 and Q_9 isolate the input stage from second-stage (predriver) loading effects and produce a combined common-mode feedback signal at the junction of R_{19} and R_{20} to properly bias Q_6 and Q_7. This also provides additional common-mode rejection by reducing the common-mode impedance seen by the collectors of the input stage. Limiter diodes D_2 and D_3 prevent excessive signal swings at the collectors of Q_4 and Q_5 when the amplifier is clipping.

Operation of this circuit can be understood by looking at what would happen if the sum of the drain currents of Q_1 and Q_2 (i.e., the common-mode current) were to increase for some reason. The collector currents of Q_4 and Q_5 would then exceed those of Q_6 and Q_7, respectively. This would cause the base voltages of Q_8 and Q_9 to go in a negative direction, in turn causing the common-mode feedback signal at the junction of R_{19} and R_{20} to go in a negative direction. As a result, the collector currents of Q_6 and Q_7 would increase by the amount necessary to equal those of Q_4 and Q_5, thus restoring balance. Notice that this common-mode feedback loop acts to keep the voltage at the junction of R_{19} and R_{20} equal to the positive rail voltage less the combined voltage drop of an emitter resistor (R_{15} or R_{16}) and a base–emitter junction (Q_6 or Q_7), If the common-mode current supplied by Q_3 were to increase by 0.1 mA, for example, this combined voltage drop would change by roughly 25 mV (primarily due to increased emitter resistor voltage drop). The common-mode voltage at the collectors of Q_4 and Q_5 would thus also change by 25 mV, implying a common-mode impedance at these nodes of 250 Ω. The effects of differential-mode current signals at the collectors of Q_4 and Q_5 sum to zero at the junction of R_{19} and R_{20}. Differential signals are thus unaffected by the common-mode feedback loop and see a high differential-mode impedance as a result.

The complementary predriver stage consists of a differential cascode (Q_{10}–Q_{13}) loaded with a Darlington-cascode current mirror (Q_{14}–Q_{17}) to provide a single-ended drive for the output stage. Notice that the operating current of the differential pair (Q_{10}, Q_{11}) is set by the common-mode voltage at the junction of R_{19} and R_{20}, which in turn is governed by the current supplied by Q_3. The cascode achieves high speed by eliminating the Miller effect and allowing the use of fast low-voltage transistors in the common-emitter differential amplifier. Elimination of the Miller effect is also important in reducing high-frequency distortion resulting from nonlinear collector–base junction capacitance [7]. The cascode configuration also improves low-frequency linearity and power supply rejection by reducing the Early effect. The complementary predriver structure, made possible by the current mirror, greatly reduces second-order distortion.

Transistors Q_{18} and Q_{19} provide regulated bias for the cascode bases and emitter–follower collectors. Adequate current is available so that these voltages remain stable even under clipping conditions. Diodes D_4–D_7 prevent the cascodes from saturating when the amplifier clips. Zener diode D_8 provides for two identical drive signals offset by 22 V to allow for biasing and error correction in the output stage.

Overall negative feedback connections and frequency compensation are also shown in Fig. 8. R_{11} and R_{12} set the closed-loop gain at approximately 20. The resistance of this divider was chosen to be fairly low to avoid noise and maintain good high-frequency characteristics. As a result, current flow and dissipation is not insignificant (100 mW in R_{12} at 50-W operating level). To avoid thermally induced distortion at low frequencies, these resistors should be oversized metal-film types, 1 and 2 W, respectively.

Feedback compensation is provided by C_4 and R_{13},

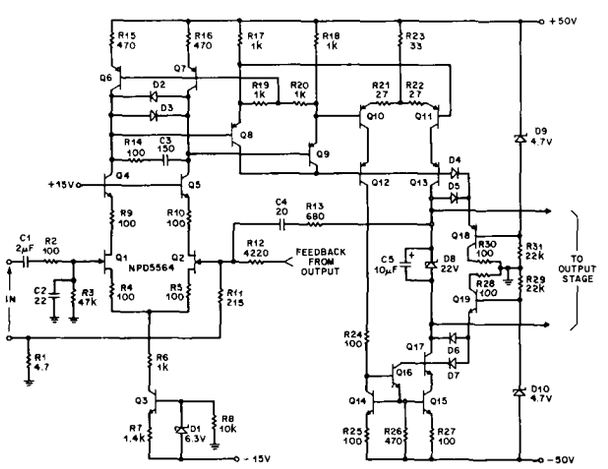


Fig. 8. MOSFET power amplifier front end. Differential cascode circuitry minimizes distortion.

which implement rolloff feedback from the output of the predriver to the inverting amplifier input, establishing a stable gain crossover frequency of about 2 MHz. Providing compensation by feedback to the input stage tends to allow improved slew rate and reduced power supply coupling, the latter because both ends of the network are ground-referenced (in contrast to the Miller-effect compensation of Fig. 7). Elements C_3 and R_{14} act to stabilize the loop formed by C_4 and R_{13}. This front-end design enables the amplifier to achieve a slew rate in excess of 300 V/μs.

2.2 Output Stage and Error Correction

In virtually any well-designed power amplifier the output stage ultimately limits performance. It is here where both high voltages and large current swings are present, necessitating larger, more rugged devices which tend to be slower and less linear over their required operating range. The performance-limiting nature of the output stage is especially true in class B and AB designs, where the signals being handled by each "half" have highly nonlinear half-wave-rectified waveforms and where crossover distortion is easily generated. In contrast, it is not difficult or prohibitively expensive to design front-end circuitry of exceptional linearity.

Overall negative feedback greatly improves amplifier performance (including dynamic distortions such as transient intermodulation distortion [7]), but it becomes progressively less effective as the frequency or speed of the errors being corrected increases. High-frequency crossover notch distortion is a good example. For this reason, several high-performance amplifier designs now employ feedforward error correction in addition to conventional negative feedback. However, some of these designs can be complex and expensive. The philosophy of this design is based on the observation that only the output stage needs extra error correction and that such local error correction can be less complex and more effective.

While the power MOSFET has many advantages, it was pointed out in Section 1.3 that the lower transconductance of the MOSFET will result in considerable crossover distortion unless rather high bias currents are chosen. Fig. 9 illustrates this effect by showing the individual and summed transconductances of both halves of a class AB MOSFET output stage as a function of net output current. At a bias current of 150 mA and a load of 8 Ω this transconductance variation can result in open-loop output stage harmonic distortion on the order of 1% as pictured in Fig. 10(a) and (b). Mismatches in the transconductance characteristics of the top and bottom output devices also contribute to the distortion of Fig. 10. Again, while bipolar transistor transconductance is high enough and consistent enough that it is relatively unimportant in an emitter–follower stage, MOSFET transconductance is smaller and less consistent, making it a significant parameter in source–follower stages.

Fig. 11 illustrates an error-correction technique described by Hawksford, which is well suited to this application [1]. Here the output stage, being a source follower, is modeled as having exactly unity gain with an error voltage $e(x)$ added. This error represents any departure from unity gain, whether it is a linear departure due to less than unity gain, a distortion due to transconductance nonlinearity, or injected errors like power supply ripple. A differential amplifier, represented by summer S_1, merely subtracts the output from the input of the power stage to arrive at $e(x)$. This error signal is then added to the input of the power stage by summer S_2 to provide that distorted input which is required for an undistorted output. Note that this is an error-cancellation technique like feedforward as opposed to an error-reduction technique like negative feedback. This technique is in a sense like the dual of feedforward. It is less expensive because the point of summation is a low-power internal amplifier node. It is less critical of component tolerances and frequency response matching because less circuitry is enclosed and that circuitry is simple. Feedforward tends to become less effective at very high frequencies because the required phase and amplitude matching for error cancellation becomes progressively more difficult to maintain. The technique of Fig. 11 also tends to become less effective at very high frequencies because, being a feedback loop (albeit not a traditional negative feedback loop), it requires some amount of compensation for stability, detracting from the phase and amplitude matching.

A schematic of the MOSFET power amplifier's output stage and error-correction circuit is shown in Fig. 12. The error-correction circuit is a slightly modified version of one illustrated in [1]. Emitter followers Q_{20} and Q_{21} isolate the high-impedance predriver output nodes from the output stage and provide a low-impedance signal for the error-correction summation process. Double emitter followers Q_{24}, Q_{26} and Q_{25}, Q_{27} provide a high-current drive capability for the MOSFET gates and isolate the error-correction summing nodes from the MOSFET gate loads. Note that Q_{24} and Q_{25} can be fast,

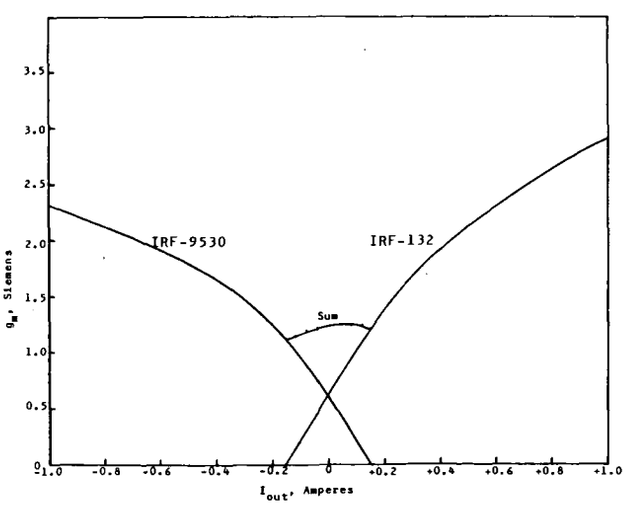


Fig. 9. Output stage transconductance versus output current (I_{bias} = 150 mA). Reduced total transconductance in central region can cause crossover distortion.

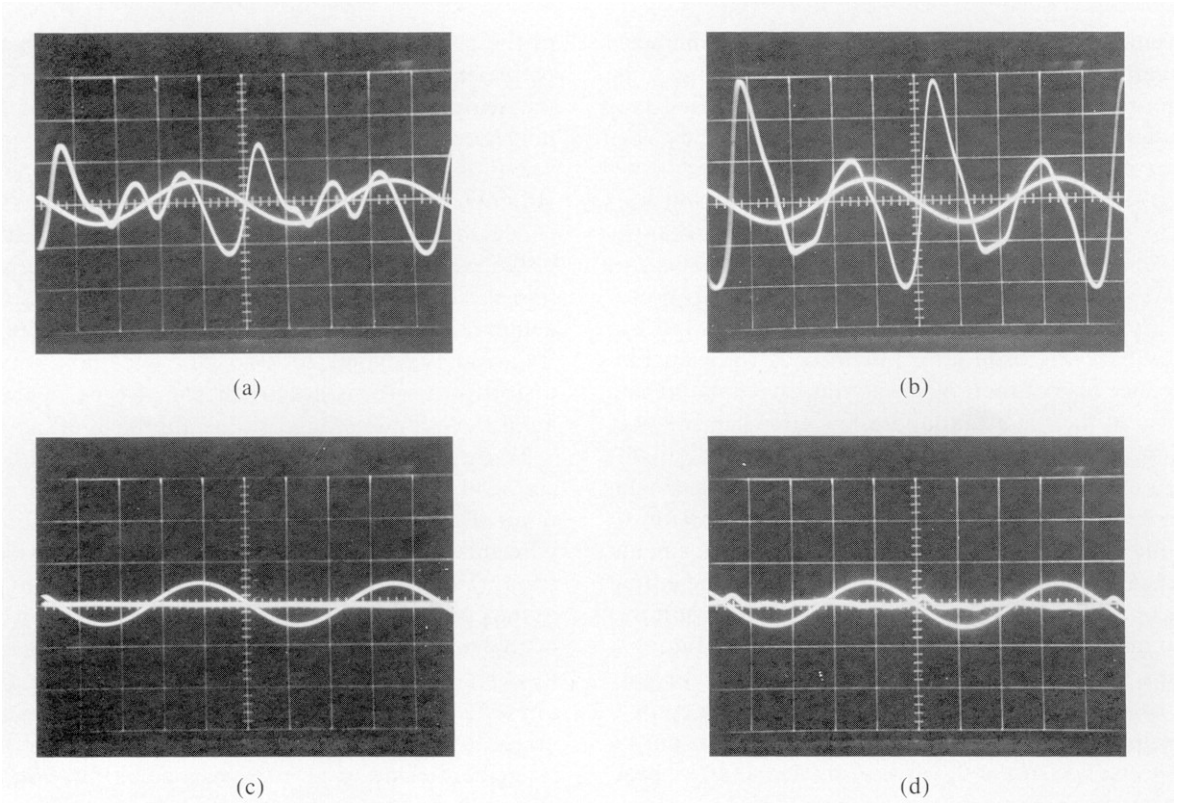


Fig. 10. Output stage open-loop distortion (THD). (a) 1 kHz, no error correction. (b) 20 kHz, no error correction. (c) 1 kHz, with error correction. (d) 20 kHz, with error correction. Vertical distortion scale 0.5%/div. All measurements at full power (50 W).

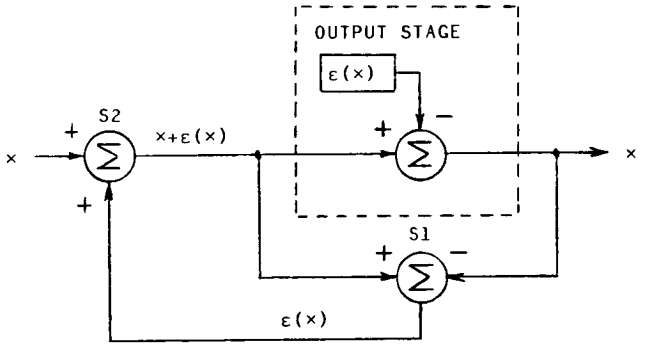


Fig. 11. Output stage error correction [1].

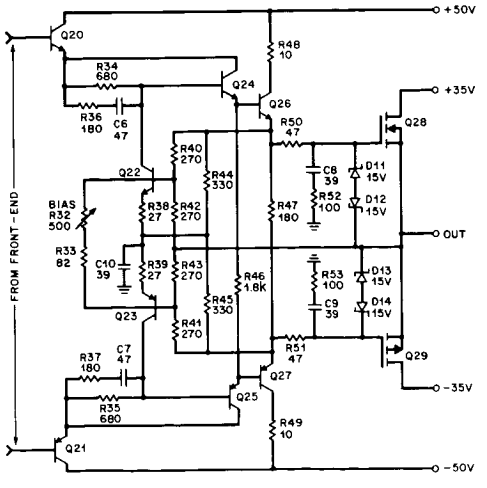


Fig. 12. MOSFET power amplifier output stage. Q_{22} and Q_{23} provide error-correction signals.

inexpensive small-signal transistors. Transistors Q_{22} and Q_{23} and resistors R_{38}–R_{45} comprise the differential amplifier for summer S_2 of Fig. 11. The output current of these transistors is summed with the input signal (summer S_2 of Fig. 11) by means of R_{34} and R_{35}. For error correction, the top and bottom halves (Q_{22}, Q_{23}) work independently to produce identical correction signals.

Input signals offset by ±11 V, as supplied by the predriver circuit, provide dc operating voltage for these circuits. These offset voltages must be adequate to allow for the maximum bias plus V_{gs} signal swing required by the MOSFETs. Transistors Q_{22} and Q_{23}, in conjunction with R_{32} and R_{33}, control the dc voltage drop across R_{34} and R_{35}. They thus set the bias for the MOSFETs by means of a V_{be}-referenced feedback loop which also includes Q_{24}, Q_{25}, Q_{26}, and Q_{27}. Transistor Q_{22} is mounted on the heat sink to provide thermal feedback. Resistors R_{38} and R_{39} control the loop gain of the bias loops and improve stability. Overall frequency compensation of the error correction and bias loops is provided by R_{36}, R_{37}, C_6, C_7, and C_{10}.

Fig. 10(c) and (d) shows open-loop distortion of the output stage with error correction to be less than 0.1%, illustrating an improvement of better than an order of magnitude, even at 20 kHz. This was achieved with 5% tolerance resistors. While use of closer tolerance resistors would improve the correction at lower frequencies, where it is unnecessary, their use would make a smaller improvement at 20 kHz because performance there is beginning to be limited by the speed of the

error-correction loop. Sensitivity of 20-kHz to tolerance in the error correction circuit has been measured to be approximately 0.0002% per percent in the closed-loop amplifier. For ultimate performance, a pot can be placed between the junctions of R_{38}, R_{39} and R_{44}, R_{45}.

The output stage is completed by C_8, C_9, and R_{50}–R_{53} for control of parasitic oscillations and D_{11}–D_{14} for protection of the MOSFET gates from excessive drive voltages. As mentioned in Section 1.6, power MOSFETs are considerably more prone to high-frequency parasitic oscillations than bipolar power transistors because of their inherent high-speed nature and because of their substantial drain–source capacitance, making it easy to form an efficient Colpitts oscillator structure with inductance in the gate circuit. The amount of series gate resistance required for suppression of parasitic oscillations grows in proportion to the amount of inductance in the gate circuit. For high-speed output stage operation it is therefore important to minimize this inductance. Although not employed in Fig. 12, this can be done especially well by shielding the gate leads back to the driver transistors, grounding the shield to the local bypass ground at each end. Then only a 10-Ω series resistor at the driver end and a ferrite bead at the gate end are necessary.

3 AMPLIFIER PERFORMANCE

This amplifier employs substantial amounts of negative feedback (40 dB at 20 kHz), and 20-kHz total harmonic distortion was the primary performance metric used in the design process. In recent years several new forms of distortion have been described, sometimes in the belief that they were caused by large amounts of negative feedback and that traditional measures of distortion (e.g., harmonic and intermodulation) would be ineffective in detecting them. Some of these beliefs have been shown to be unfounded [7]–[15]. Nevertheless it was decided to include some of these newer measures of distortion in the performance evaluation.

In spite of the error correction, which improves performance by more than an order of magnitude, transconductance variation in the output stage is still the dominant source of distortion in this amplifier. For this reason, output stage bias current continues to influence performance, and tradeoffs can be made. The measurements presented here were made at a bias current of 150 mA, resulting in a quiescent output stage power dissipation of 11 W for the 50-W amplifier. It should also be noted that the transconductance characteristics of the *n*- and *p*-channel output devices were not matched.

3.1 Measurement Technique

A word about measurement technique is in order. In many cases the distortions being measured were below those levels measurable by conventional equipment and techniques. In order to add dynamic range to that provided by the equipment employed, a distortion magnifier circuit was utilized.

The distortion magnifier circuit scales the output level of the noninverting amplifier under test down to that of the input, subtracts the two, reintroduces 11% of the scaled-down amplifier output signal, and finally multiplies the result by 9 for presentation to the measuring equipment. The net effect is to provide unity gain for the fundamental and a gain of 10 to distortion products generated by the amplifier under test. Amplitude and phase balance adjustments were incorporated into the output signal path prior to the subtraction to achieve a fundamental null of greater than 60 dB to frequencies beyond 20 kHz. The excellent noise and distortion performance of the 5534-type operational amplifiers employed make this approach effective.

To measure harmonic distortion, for example, a sensitive THD analyzer [16] with a 20-kHz measurement floor of about 0.001% was employed in combination with this distortion magnifier to achieve a residual of about 0.0003% at 20 kHz, primarily limited by noise of the power amplifier under test. The distortion output of the analyzer was then observed with both an oscilloscope and a spectrum analyzer. The latter further improves the measurement floor in most cases. Most of the other distortion tests employed a similar arrangement. Due to an oscilloscope calibration error, all vertical deflections in the figures are 6.4% low.

3.2 Harmonic and SMPTE Intermodulation Distortion

Figs. 13 and 14 show total harmonic distortion as a function of frequency and power. Dashed portions of the curves indicate that distortion is below the residual of the measuring system. Fig. 15 shows the appearance of the 20-kHz full-power harmonic distortion products without and with output stage error correction. Fig. 16 illustrates a virtually unmeasurable level of SMPTE[1] intermodulation distortion (60 and 7000 Hz, 4:1).

3.3 Transient Intermodulation Distortion

Dynamic intermodulation distortion, a test for measurement of transient intermodulation distortion, is

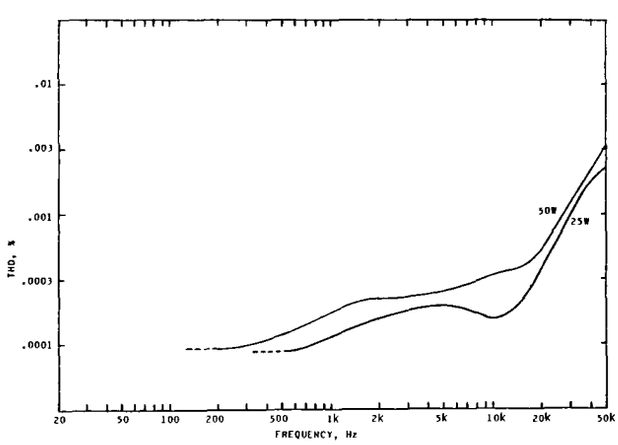


Fig. 13. Total harmonic distortion as a function of frequency.

[1] Society of Motion Picture and Television Engineers.

shown in Fig. 17 [17]. In this test a 3.18-kHz square wave and a 15-kHz sine wave are mixed 4:1 and passed through the amplifier. A spectrum analyzer is used to measure the in-band intermodulation components. Performance is shown for both 30-kHz and 100-kHz first-order low-pass filtering of the square-wave source (DIM-30 and DIM-100). As predicted by the good 20-kHz total harmonic distortion performance and high slew rate of this amplifier, both DIM-30 and DIM-100 distortion levels are very low; in fact, the former is unmeasurable.

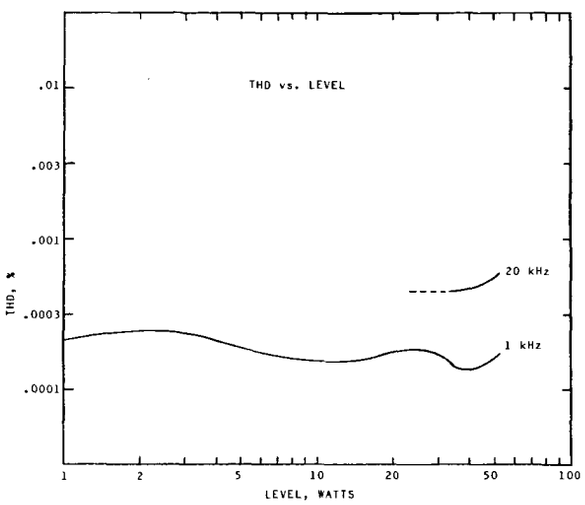


Fig. 14. Total harmonic distortion as a function of level.

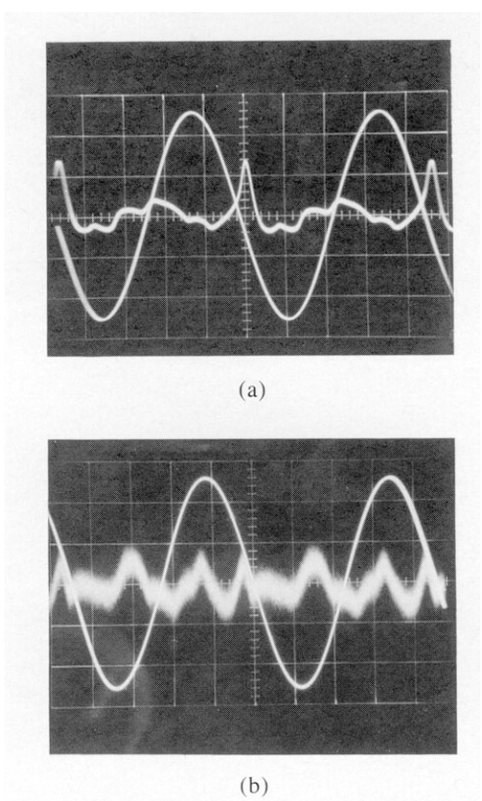


Fig. 15. 20-kHz total harmonic distortion products at full power (50 W). (a) Without error correction (THD analyzer reads 0.02%). (b) With error correction (THD analyzer reads 0.0006%).

3.4 Interface Intermodulation Distortion

Interface intermodulation distortion [12], [13], [18] is measured by applying 1000 Hz to the amplifier under test and 60 Hz to a test amplifier, each of which drives opposite ends of an 8-Ω load resistor. A spectrum analyzer is then used to measure distortion products at the output of the amplifier under test. Both amplifiers are operated at half the rated power of the amplifier under test, and distortion products are referred to the 1-kHz level at the output of the amplifier under test. For this test the spectrum analyzer was preceded by a modified version of the distortion magnifier to produce a magnification of 100. Interface intermodulation distortion was unmeasurable, at less than 0.0001%.

3.5 Phase Intermodulation Distortion

Phase intermodulation distortion is shown in Fig. 18 [14], [15], [19]. It is measured in the same way as SMPTE intermodulation, except that phase modulation of the carrier is measured instead of amplitude modulation. The phase modulation is then expressed in time (e.g., rms nanoseconds) [14].

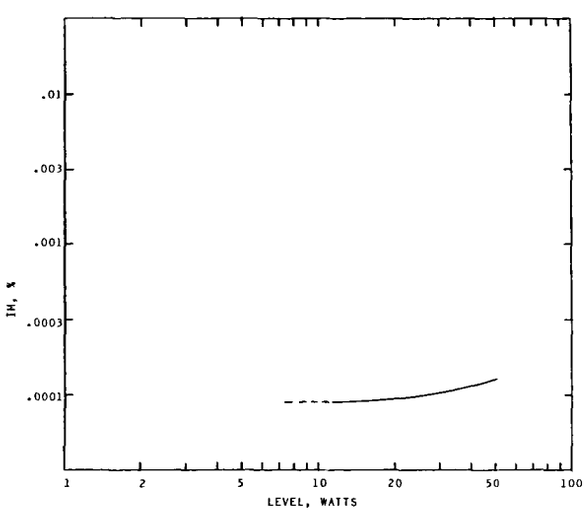


Fig. 16. SMPTE intermodulation distortion as a function of level.

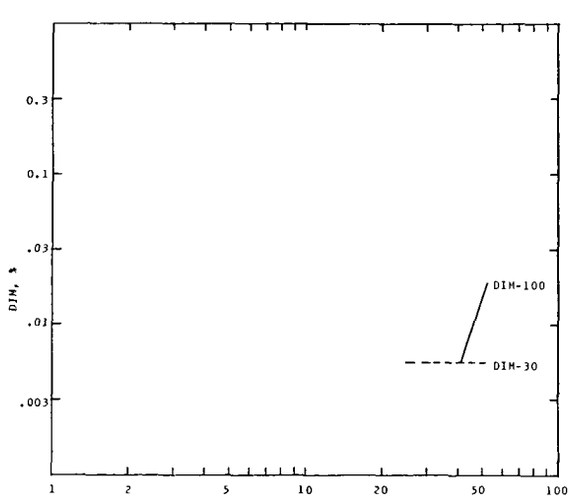


Fig. 17. Dynamic intermodulation distortion (DIM-30 and DIM-100) as a function of level.

3.6 Damping Factor

The damping factor as a function of frequency is shown in Fig. 19 and is extremely high. It is high for three reasons: 1) the power MOSFETs present very light loading to the drivers, producing a low open-loop output impedance essentially equal to the inverse of their transconductance; 2) the error correction circuit tends to drive this open-loop output impedance to zero; 3) substantial overall negative feedback further reduces the output impedance by an amount approximating the feedback factor (40 dB at 20 kHz). Inclusion of a parallel *R-L* network (0.5 Ω, 0.5 μH) at the output in series with the load for complete capacitive load stability will reduce the high-frequency damping factor to 125 at 20 kHz.

Although the need for this much damping factor is doubtful, the importance of the damping factor on the frequency response and coloration has sometimes been underestimated. This is explained by the fact that most loudspeaker systems are designed assuming that they will be driven by a pure voltage source (sometimes, it seems, with limitless current capability as well!). For example, the impedance of a nominal 4-Ω system may dip to 2.5 Ω and rise to over 50 Ω at various points across the frequency band due to driver and crossover resonances. A typical bipolar amplifier may have a damping factor of 100 (often less at high frequencies), resulting in frequency response deviations on the order of 0.3 dB with such a load. Coloration due to low damping factor may also partly explain audible differences among vacuum-tube and low-feedback designs.

3.7 Peak Output Current

While the damping factor identifies the degree of control an amplifier has over its load in a small-signal sense, the output current capability determines the degree to which that control will be enforced under large-signal conditions. A large output current capability is made necessary by many of the same factors mentioned above which make a high damping factor important. Reactive energy stored in loudspeakers can result in especially serious current demands being placed on amplifiers when the loudspeaker is excited with certain signals. For example, in [12] it is shown that an ordinary closed-box woofer alone can demand as much as 2.5 times the peak current of a similarly rated resistive load. Recent experimental data from real multiway systems confirm this and demonstrate that simultaneous excitation of multiple drivers serving different frequency ranges can lead to even larger ratios, in the range of 3–6 [20].

Output current is another area in which power MOSFETs can excel. Fig. 20 shows a 2-cycle tone burst at 20 kHz with a 1% duty cycle being driven into a 1-Ω load resistor by this amplifier. It illustrates a peak current of over 22 A. This is an extremely high current capability for a 50-W amplifier with only one output transistor of each polarity. The use of a 20-kHz tone burst reduces the effect of power supply sag and also serves to illustrate that current slew-rate limiting does not occur

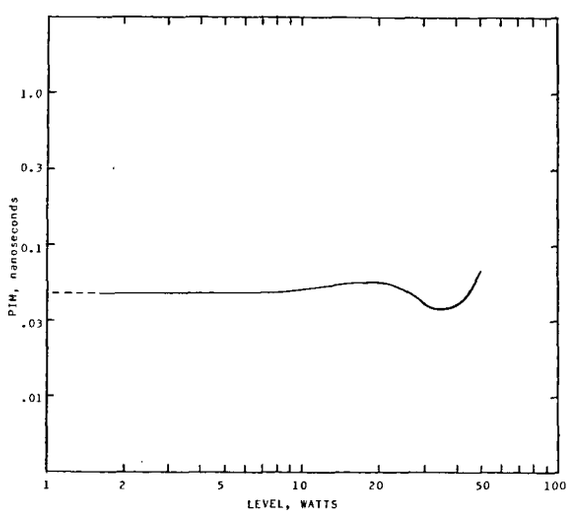


Fig. 18. Phase intermodulation distortion as a function of level. Note that phase modulation is expressed in rms nanoseconds.

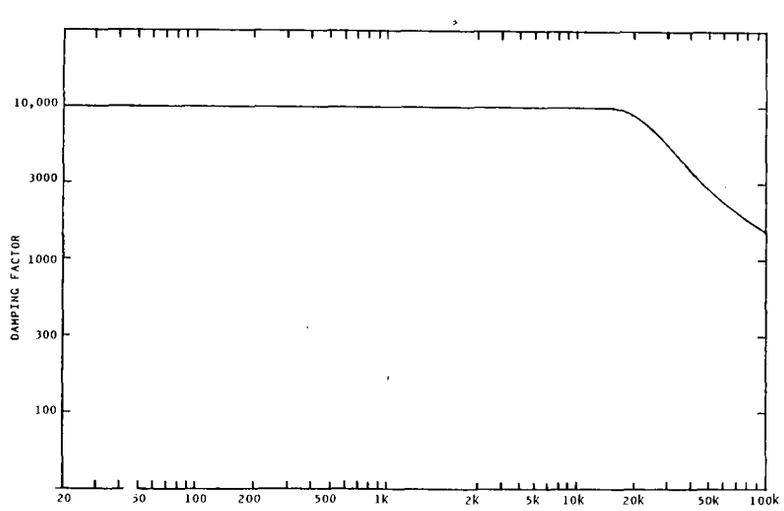


Fig. 19. Damping factor as a function of frequency.

even at this very high rate of current change. A similar test into a 0.5-Ω load exhibited undistorted tone bursts up to peak currents of 35 A. Higher frequency tests yielded undistorted current slopes in excess of 30 A per microsecond. The amplifier also performed satisfactorily with a 20-Hz tone burst into a 1-Ω load, but the effect of power supply sag was in much greater evidence, reducing the peak current to 18 A.

3.8 Square Waves and Reactive Loads

Fig. 21 illustrates small-signal and full-power 20-kHz square waves into an 8-Ω load. Fig. 22 shows small-signal and full-power 20-kHz square waves into a reactive load consisting of 1 Ω and 1 μF in series. In the full-power case the square wave has been band-limited to 200 kHz by a first-order low-pass filter. Fig. 23 shows 500-kHz small-signal square waves into an 8-Ω resistive load and a reactive load consisting of 1 Ω and 1 μF in series. It also shows a full-power 500-kHz square wave into an 8-Ω load. Few bipolar amplifiers would survive this test. Table 1 summarizes overall performance of the amplifier.

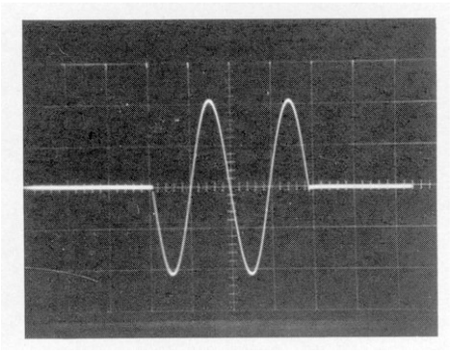
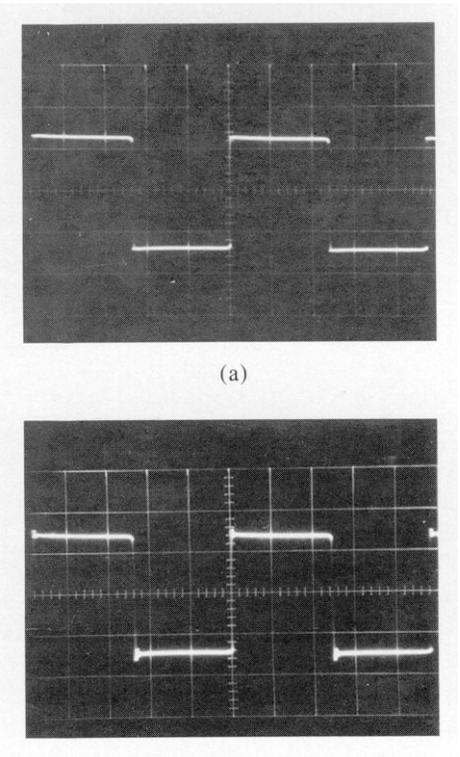


Fig. 20. 2-cycle toneburst at 20 kHz into a 1-Ω resistive load illustrating peak output current capability of over 22 A. (10 V/div).



(a)

(b)

Fig. 21. 20-kHz square wave into an 8-Ω load. (a) Small signal (1 V/div). (b) Full power (20 V/div).

4 CONCLUSION

Power MOSFETs are capable of exceptional performance when used in combination with good drive circuitry and simple error-correction circuitry. Their ability to operate without complex and unreliable safe-area limiting circuitry makes them especially useful for demanding audio applications. Compared with bipolar transistors, the major disadvantage of MOSFETs (and source of distortion) seems to be the lower transconductance, but this can be dealt with effectively by means of a simple error-correction circuit. Although a MOSFET power amplifier can still be expected to cost a little more, the improved characteristics seem to justify the small premium in applications where performance is important.

5 REFERENCES

[1] M. J. Hawksford, "Distortion Correction in Audio Power Amplifiers," presented at the 65th Convention of the Audio Engineering Society, *J. Audio Eng. Soc. (Abstracts)*, vol. 28, pp. 364–366 (1980 May), preprint 1574.

[2] *Hitachi Power MOSFET Data Book HLN600* (Hitachi America, Ltd., 1983).

[3] *International Rectifier HEXFET Databook* (International Rectifier Corporation, 1981).

[4] T. Sato, K. Higashiyama, and H. Jiko, "Amplifier Transient Crossover Distortion Resulting from Temperature Change in the Output Power Transistors," presented at the 72nd Convention of the Audio Engineering Society, *J. Audio Eng. Soc. (Abstracts)*, vol. 30, pp. 949, 950 (1982 Dec.), preprint 1896.

[5] E. S. Oxner, "Analyzing and Controlling the Tendency for Oscillation of Parallel Power MOSFETs," *Proc. Powercon*, vol. 10 (1983 Mar.).

[6] T. Holman, "New Factors in Power Amplifier Design," *J. Audio Eng. Soc. (Engineering Reports)*, vol. 29, pp. 517–522 (1981 July/Aug.).

[7] R. R. Cordell, "Another View of TIM," *Audio*, vol. 64 (1980 Feb., Mar.).

[8] W. G. Jung, M. L. Stephens, and C. C. Todd, "An Overview of SID and TIM," *Audio*, vol. 63 (1979 June-Aug.).

[9] P. Garde, "Transient Distortion in Feedback Amplifiers," *J. Audio Eng. Soc.*, vol. 26, pp. 314–322 (1978 May).

[10] E. M. Cherry, "Transient Intermodulation Distortion; Part I—Hard Nonlinearity," *IEEE Trans. Acoust., Speech, Signal Proc.*, vol. ASSP-29, pp. 137–146 (1981 Apr.).

[11] R. R. Cordell, "A Fully In-Band Multitone Test for Transient Intermodulation Distortion," *J. Audio Eng. Soc.*, vol. 29, pp. 578–586 (1981 Sept.).

[12] R. R. Cordell, "Open-Loop Output Impedance and Interface Intermodulation Distortion in Audio Power Amplifiers," presented at the 64th Convention

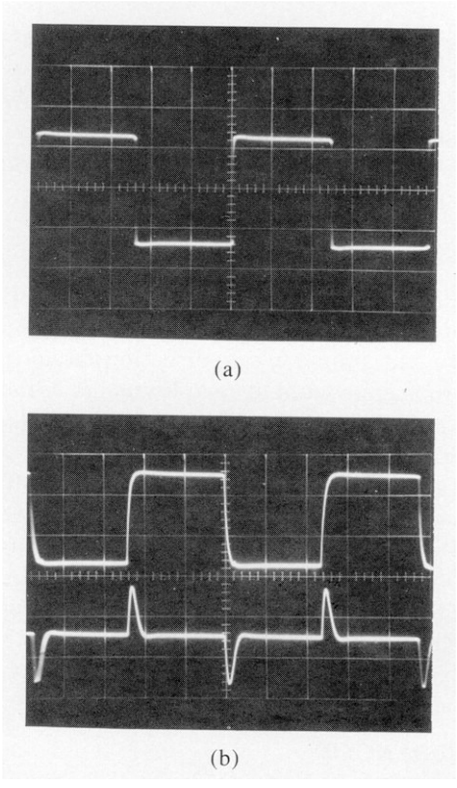


Fig. 22. 20-kHz square wave into a 1-Ω resistor in series with a 1-μF capacitor. (a) Small signal (1 V/div). (b) Full power (input bandlimited to 200 kHz). Top trace—20 V/div; bottom trace—output current at 20 A/div, time-base—10 μs/div.

Table 1. Summary of MOSFET power amplifier performance.

Power output (R_L = 8 Ω)	50 W
Total harmonic distortion, 20 Hz to 20 kHz	<0.001%
SMPTE intermodulation distortion	0.00013%
Dynamic intermodulation distortion	
DIM-30	<0.006%*
DIM-100	0.014%
Interface intermodulation distortion (IIM)	0.0001%
Phase intermodulation distortion (PIM)	<0.1 ns
Slew rate	>300 V/μs
Rise time	100 ns
Damping factor, 20 Hz to 20 kHz	>5000
Signal-to-noise ratio, A-weighted, re 1 W	108 dB

* Below measurement floor.

of the Audio Engineering Society, *J. Audio Eng. Soc. (Abstracts)*, vol. 27, p. 1022 (1979 Dec.), preprint 1537.

[13] E. M. Cherry and G. K. Cambrell, "Output Resistance and Intermodulation Distortion of Feedback Amplifiers," *J. Audio Eng. Soc.*, vol. 30, pp. 178–191 (1982 Apr.).

[14] R. R. Cordell, "Phase Intermodulation Distortion—Instrumentation and Measurements," *J. Audio Eng. Soc.*, vol. 31, pp. 114–124 (1983 Mar.).

[15] E. M. Cherry, "Amplitude and Phase of Intermodulation Distortion," *J. Audio Eng. Soc.*, vol. 31,

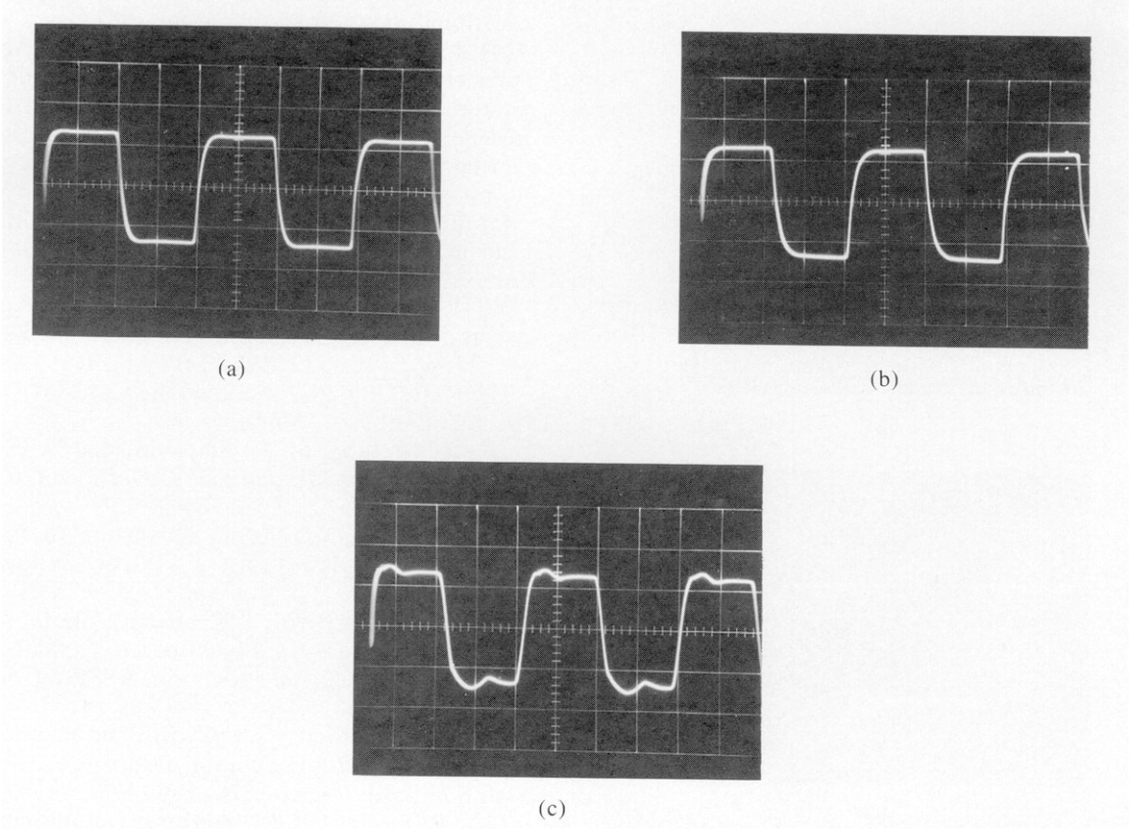


Fig. 23. 500-kHz square wave response. (a) Small signal, 8-Ω load (1 V/div). (b) Small signal, 1 Ω and 1 μF series load (1 V/div). (c) Full power, 8-Ω load (20 V/div). Time base—0.5 μs/div.

pp. 298–304 (1983 May).

[16] R. R. Cordell, "Build a High-Performance THD Analyzer," *Audio*, vol. 65 (1981 July-Sept.).

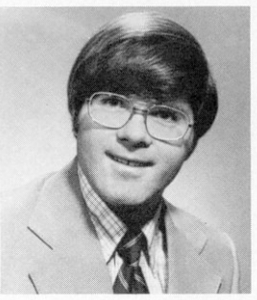
[17] E. Leinonen, M. Otala, and J. Curl, "A Method for Measuring Transient Intermodulation Distortion (TIM)," *J. Audio Eng. Soc.*, vol. 25, pp. 170–177 (1977 Apr.).

[18] M. Otala and J. Lammasniemi, "Intermodulation Distortion in the Amplifier–Loudspeaker Interface," presented at the 59th Convention of the Audio Engineering Society, *J. Audio Eng. Soc. (Abstracts)*, vol. 26, p. 382 (1978 May), preprint 1336.

[19] M. Otala, "Feedback-Generated Phase Nonlinearity in Audio Amplifiers," presented at the 65th Convention of the Audio Engineering Society, *J. Audio Eng. Soc. (Abstracts)*, vol. 28, p. 366 (1980 May), preprint 1576.

[20] I. Martikainen, A. Varla, and M. Otala, "Input Current Requirements of High-Quality Loudspeaker Systems," presented at the 73rd Convention of the Audio Engineering Society, *J. Audio Eng. Soc. (Abstracts)*, vol. 31, p. 364 (1983 May), preprint 1977.

THE AUTHOR



Robert R. Cordell received a B.S. degree from Rensselaer Polytechnic Institute, Troy, NY, in 1970 and an M.S. degree from Stanford University, Stanford, California, in 1971, both in electrical engineering.

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